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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/723,348 | 11/27/2000 | Jean-Francois Link | 00-RO-266 | 5977 |

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| EXAMINER | |
|---|---|
| DINH, MINH | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2132 | |

DATE MAILED: 07/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/723,348 | LINK ET AL. | |
| | Examiner | Art Unit | |
| | Minh Dinh | 2132 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-36 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-36 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-36 have been examined.

### *Specification*

2. The abstract of the disclosure is objected to because: it contains more than one paragraph; "Fig. 3" (line 31) should be removed. Correction is required.

### *Claim Objections*

3. Claims 2, 9, 11, 14, 21, 28, 32 and 36 are objected to because of the following informalities:

a. Regarding claims 2 and 21, insert "of" between "validity" and "all" (3rd line).

b. Regarding claims 9 and 28, insert "to" after "response" (3rd line of claim 9 and 2nd line of claim 28).

c. Regarding claim 11, insert "for" after "gating means" (4th line).

d. Regarding claim 14, insert "for" after "selection means" (3rd line); remove the comma (,) after "selection signal" (4th line).

e. Regarding claim 32, insert "the step of" after "comprising" (1st line).

f. Regarding claim 36, this claim is a method claim and cannot be dependent on claim 1, a device claim. The claim is interpreted as being dependent on claim 20.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 11 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. Regarding claim 11, it recites the limitation "reset means" in the first line. There is insufficient antecedent basis for this limitation in the claim.

b. Regarding claim 26, it is not clear what the feature "the step of from said first mode" (2nd line) is. For examination purposes, the feature is interpreted as "the step of exiting from said first mode" (see specification, page 22, lines 25-28).

### *Claim Rejections - 35 USC § 102*

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-3, 6-8, 17-18, 20-22, 25-27 and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Dornier (5,646,535).

a. Regarding claims 1, which is representative of claim 20, Dornier discloses a device containing protected data, comprising:

memory means for storing protected data (col. 3, lines 52-55);

checking means, operative in a first mode, for checking the validity of said data and for producing a validity signal enabling to determine whether said data is valid (col. 3, lines 52-55).

Dornier does not explicitly disclose validity signal output control means for inhibiting an output of said validity signal to outside said device until the validity of a predetermined quantity of said protected data has been checked. However, this feature is deemed to be inherent to the Dornier device as lines 55-62 of column 3 shows that the validity signal is not output until the BIOS checksum is completed. The Dornier device would be inoperative if there were no control means for inhibiting the output of the validity signal until the validity of the ROM BIOS has been checked.

b. Claims 2-3, 6-8, 21-22 and 25-27 are rejected on the same basis as claims 1 and 20.

c. Regarding claim 17, Dornier further discloses that the memory means is a read-only memory (col. 3, lines 52-55).

d. Regarding claims 18 and 35, Dornier further discloses that the protected data comprises program code (col. 3, lines 52-55).

8. Claims 1-8, 17-18, 20-27, 32 and 35 are rejected under 35 U.S.C. 102(e) as being anticipated by Langford et al. (6,470,450).

a. Regarding claim 1, which is representative of claim 20, Langford discloses a device containing protected data, comprising:

memory means for storing said protected data (col. 4, lines 4-7);

checking means, operative in a first mode, for checking the validity of said data and for producing a validity signal enabling to determine whether said data is valid; the validity signal being a checksum value (col. 3, lines 10-15; col. 4, lines 26-34).

Langford does not explicitly disclose validity signal output control means for inhibiting an output of said validity signal to outside said device until the validity of a predetermined quantity of said protected data has been checked. However, this feature is deemed to be inherent to the Langford device as lines 55-63 of column 7 show that the validity signal is not output until the validity of the application has been checked. The Langford device would be inoperative if there were no control means for inhibiting the output of the validity signal until the validity of the application has been checked.

b. Claims 2-8, 21-27 and 32 are rejected on the same basis as claim 1.

c. Regarding claim 17, Langford further discloses that the memory means is a ROM (col. 4, lines 4-7).

d. Regarding claims 18 and 35, Langford further discloses that the protected data comprises program code (col. 4, lines 4-7).

***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 9-10, 12, 14-15, 28-29, 31 and 33-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Langford as applied to claim 1 above, and further in view of Noll (6,185,696).

a. Regarding claims 9 and 28, Langford does not disclose that the device comprises reset means for resetting the checking means in response to a device reset in the first mode. Noll discloses reset means for resetting checking means in response to a system reset which meets the limitation of a device reset (col. 1, lines 34-41; col. 4, lines 11-23; col. 6, lines 6-10). It would have been obvious to one of ordinary skill in the art at the time the invention was made modify the Langford device such that the device comprises reset means for resetting the checking means in response to a device reset, as taught by Noll. The motivation for doing so would have been to prevent possible system malfunctions upon system resets due to errors in the BIOS ROM.

b. Regarding claims 10 and 29, Langford does not disclose that the device comprises means for exiting from the first mode upon a device reset. Noll discloses means for exiting from the first mode upon a system reset which meets the limitation of a device reset (col. 1, lines 34-41; col. 4, lines 11-23). It would have been obvious to

one of ordinary skill in the art at the time the invention was made modify the Langford device such that the device comprises reset means for resetting the checking means in response to a device reset, as taught by Noll. The motivation for doing so would have been to prevent possible system malfunctions upon system resets due to errors in the BIOS ROM.

c. Regarding claims 12 and 31, Langford does not disclose reset means operative to reset the validity signal upon the device being force to leave the first mode prematurely. Noll discloses reset means operative to reset the validity signal upon a system reset (col. 1, lines 34-41; col. 4, lines 11-21). It would have been obvious to one of ordinary skill in the art at the time the invention was made modify the Langford device such that the device comprises reset means operative to reset the validity signal upon a system reset, as taught by Noll; the system reset forces the device to leave the first mode prematurely. The motivation for doing so would have been to prevent possible system malfunctions at system resets due to errors in the BIOS ROM.

d. Regarding claims 14 and 33, Langford does not disclose that the memory means comprises a chip enable input, the input being connected to selection means for delivering an enable signal when a first mode selection signal and a protection option signal are active. Noll discloses that the memory means comprises a chip enable input, the input being connected to selection means for delivering an enable signal when a first mode selection signal a protection option signal are active (col. 3, lines 29-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made modify the Langford device such that the memory means comprises a chip

enable input, the input being connected to selection means for delivering an enable signal when a first mode selection signal and a protection option signal are active, as taught by Noll. The motivation for doing so would have been to selectively enable and disable the primary BIOS ROM and the secondary BIOS ROM.

e. Regarding claims 15 and 34, Langford discloses that an address belonging to the memory means is selected at an address input in order to enable the memory means (col. 4, lines 9-11).

11. Claims 11 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Langford in view of Noll as applied to claims 10 and 29 above, and further in view of Jablon et al. (5,421,006). The limitation "said reset means" in claim 11 is interpreted as "reset means". Noll discloses reset means (col. 1, lines 34-41; col. 4, lines 11-23; col. 6, lines 6-10). However, Langford and Noll do not disclose that the reset means comprises latching means for temporarily latching a logic state indicating the presence of the first mode and gating means for transferring the device reset signal to a reset input of the checking means only when said logic state is present in the latching means, the latching means temporarily maintaining said gating means enabled after a caused by the device disappearance of the reset signal logic state. Jablon discloses a device for assessing the integrity of computer system software which includes reset means; the reset means comprising latching means and gating means (Abstract and fig. 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made modify the device of Langford and Noll such that the reset means comprises

latching means and gating means, as taught by Jablon; accordingly, the latching means if for temporarily latching a logic state indicative of the presence of said first mode, and the gating means is for controllably passing said device reset signal to a reset input of said checking means when said logic state is latched. The motivation for doing so would have been to protect the codes in the non-volatile memory from being overwritten by subsequent untrusted programs.

12. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Langford as applied to claim 1 above, and further in view of Tanenbaum ("Structured Computer Organization"). Langford does not disclose explicitly that the validity signal output control means is implemented in hardware. Tanenbaum teaches that hardware and software are logically equivalent and that any operation performed by software can also be built directly into hardware (page 10, "A central theme of this book ... make different decisions."). It is obvious to one of ordinary skill in the art at the time the invention was made that the Langford validity signal output control means can be implemented in hardware, as taught by Tanenbaum. The decision to put certain functions in the hardware could be made according to the system requirements.

13. Claims 16, 19 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Langford as applied to claim 1 above, and further in view of Grimmer, Jr. et al. (5,737,760). Langford does not disclose that the device is implemented in a microcontroller unit. Grimmer discloses a microcontroller unit comprising or a CPU,

volatile and nonvolatile memory (col. 1, lines 22-29). It would have been obvious to one of ordinary skill in the art at the time the invention was made modify the Langford device such that the device is implemented in a microcontroller unit, as taught by Grimmer, so that the CPU need not access off-chip memory often to operate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Dinh whose telephone number is 703-306-5617. The examiner can normally be reached on Mon - Fri: 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on 703-305-1830. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Minh Dinh
Examiner
Art Unit 2132

MD
7/8/2004

JUSTIN T. DARROW
PRIMARY EXAMINER